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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,592	02/09/2004	Byung Park	06847.P001	1757

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EXAMINER	
WYATT, KEVIN S	

ART UNIT	PAPER NUMBER
2878	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,592	PARK ET AL.	
	Examiner	Art Unit	
	Kevin Wyatt	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *23-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group 1 (claims 1-22) in the reply filed on 111/11/2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

2. Claims 23-29 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 11/16/2005.

Drawings

3. The drawings are objected to because reference numbers, figures, and figure numbers are hand written. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either

"Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-2, 4,6-7, 9-17 and 20-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Merrill (Publication No. U.S. 2002/0036700 A1).

Regarding claim 1, Merrill shows in Fig. 8, a photodetecting array (320, i.e., 2 by 2 portion of array) comprising: a plurality of detecting cells (active pixel sensors, paragraph 0047, lines 1-2) arranged in an array; a staircase grid (traced from PIX-VCC to active pixel having row-select (322-4)) of bias lines (PIX-VCC) coupled to said plurality of detecting cells (paragraph 0053, lines 1-4); a plurality of gate lines coupled to said plurality of detecting cells (324-1 and 324-2, i.e., first and second row-select lines,

paragraph 0049, lines 1-5); and a plurality of data lines (326-1 and 326-2, i.e., column out lines) coupled to said plurality of detecting cells (paragraph 0050, lines 1-7).

Regarding claim 2, Merrill shows in Fig. 3, each of said plurality of detecting cells (110, i.e., active pixel cell sensor) comprises a transistor (116, 120,126, 130, 138, 144, or 148) and a photodiode (112), and wherein one of said plurality of gate lines is coupled to said transistor and one of said plurality of data lines is coupled to said diode (paragraph 0028 lines 17-19 and paragraph 0026, lines 6-8).

Regarding claim 4, Merrill shows in Figs. 3 and 8, that each photodiode (112) in said array is segmented from other photodiodes in said array (according to paragraph 0026 lines 3-4, there is only one photodiode per active pixel sensor).

Regarding claim 6, Merrill shows in Fig. 8, that said staircase grid comprises: a first bias line (PIX-VCC line to active pixel sensor pertaining to row-select 322-1) parallel to a first gate line (324-1, i.e., row-select) of said plurality of gate lines; a second bias line (PIX-VCC line to active pixel sensor pertaining to row-select 322-3) parallel to a second gate line (324-2, i.e., row-select) of said plurality of gate lines; a third bias line (PIX-VCC line to active pixel sensor pertaining to row-selects 322-2 and 322-4) parallel to a first data line (326-1, i.e., column out) of said plurality of data lines, said third bias line being electrically coupled between said first bias line and said second bias line.

Regarding claim 7, Merrill shows in Fig. 8, that said staircase grid comprises: a first bias line (PIX-VCC line to active pixel sensor pertaining to row-select 322-1) parallel and proximate to a first gate line (324-1, i.e., row-select) of said plurality of gate lines; a second bias line (PIX-VCC line to active pixel sensor pertaining to row-select 322-3)

parallel and proximate to a second gate line (324-2, i.e., row-select) of said plurality of gate lines; a third bias line (PIX-VCC line to active pixel sensor pertaining to row-selects 322-2 and 322-4) parallel to and adjacent to a first data line (326-1, i.e., column out) of said plurality of data lines, said third bias line being electrically coupled between said first bias line and said second bias line.

Regarding claim 9, Merrill shows in Figs. 3 and 8, that said staircase grid comprises a first plurality of bias lines (PIX-VCC line to active pixel sensor pertaining to row-selects 322-1 and 322-3) which are parallel to and proximate to corresponding gate lines (324-1 and 324-2, i.e., row-selects) and a second plurality of bias lines (PIX-VCC line to active pixel sensor pertaining to row-selects 322-2 and 322-4) which are parallel to and proximate to only a portion of said plurality of data lines (portion of column out lines (326-1 and 326-2) leading directly from column out terminal of active pixel sensor) said second plurality of bias lines being coupled electrically between said first plurality of bias lines.

Regarding claim 10, Merrill shows in Fig. 3 a capacitive coupling (capacitor (136) within each pixel) between said second plurality of bias lines (132, i.e., bias potential line) and said plurality of data lines (152, i.e., column out line) is limited substantially to said portion (capacitive coupling takes place within active pixel sensor, paragraph 0029, lines 1-7 and paragraph 0031, lines 3-4).

Regarding claim 11, Merrill shows in Figs. 3 and 8, a photodetecting device comprising: a first row of detecting cells (322-1 and 322-2, i.e., active pixel cells), each having a transistor (116, 120,126, 130, 138, 144, or 148) and a photodiode (112); a

second row of detecting cells, each having a transistor (116, 120,126, 130, 138, 144, or 148) and a photodiode (112), said second row being adjacent to and parallel with said first row; a first gate line (324-1, row-select) coupled to said first row; a second gate line (324-2, row-select) coupled to said second row; a first bias voltage line (PIX-VCC line to active pixel sensor pertaining to row-selects 322-1 and 322-2) parallel with and proximate to said first gate line (324-1, row-select) and coupled to detecting cells in said first row (322-1 and 322-2, i.e., active pixel cells); a second bias voltage line (PIX-VCC line to active pixel sensor pertaining to row-selects 322-3 and 322-4) parallel with and proximate to said second gate line (324-1, row-select) and coupled to detecting cells in said second row (322-3 and 322-4, i.e., active pixel cells).

Regarding claim 12, Merrill shows in Fig. 3, said first and said second bias voltage lines provide a reverse bias voltage (132, i.e., bias potential line, paragraph 0028, lines 5-7) to photodiodes in said first row of detecting cells and in said second row of detecting cells.

Regarding claim 13, Merrill shows in Fig. 8, a third bias voltage line parallel with and proximate to a first data line, said third bias voltage line being electrically coupled between said first bias voltage line and said second bias voltage line (paragraph 0053, lines 3-4). Paragraph 0046, lines 3-7, suggests that additional pixels could be added to each column or row depending on which size required. Therefore a third bias line could be added to accommodate additional pixels in either row (which would more appropriately placed between first and second bias lines) without altering the structure of the array or departing from the concept of the invention.

Regarding claim 14, Merrill shows in Fig. 8, a second data line; a fourth bias voltage line parallel with and proximate to said second data line, said fourth bias voltage line being electrically coupled to said second bias voltage line and to a fifth bias voltage line (paragraph 0053, lines 3-4). Paragraph 0046, lines 3-7, suggests that additional pixels could be added to each column or row depending on which size required. Therefore a fourth bias line (coupled to first and fifth bias lines) could be added to accommodate additional pixels in either column or row without altering the structure of the array or departing from the concept of the invention.

Regarding claim 15, said first data (326-1, i.e., column out) line and said second data line (326-2, i.e., column out) are substantially perpendicular to said first gate line (324-1, row-select) and to said second gate line (324-2, row-select) and wherein said third bias voltage line is not coupled to said fifth bias voltage line and wherein said fourth bias voltage line is not coupled to said first bias voltage line (paragraph 0053, lines 3-4).

Regarding claim 16, Merrill shows in Fig. 8, that said first gate line (324-1, row-select) is coupled to transistors in said first row of detecting cells (322-1 and 322-2, i.e., active pixel cells) and said second gate line (324-2, row-select) is coupled to transistors in said second row of detecting cells (322-3 and 322-4, i.e., active pixel cells).

Regarding claim 17, Merrill shows in Fig. 3, that each photodiode in said first row and in said second row of detecting cells is segmented from other photodiodes.

Regarding claim 20, Merrill shows in Fig. 8 a photodetecting array (320, i.e., 2 by 2 portion of array) comprising: a plurality of detecting cells (active pixel sensors,

paragraph 0047, lines 1-2) arranged in an array, each of said detecting cells comprising a photodiode (112); a plurality of gate lines (324-1 and 324-2, i.e., first and second row-select lines, paragraph 0049, lines 1-5) coupled to said plurality of detecting cells; a plurality of data lines (326-1 and 326-2, i.e., column out lines) coupled to said plurality of detecting cells (paragraph 0050, lines 1-7); a mesh of bias voltage lines (PIX-VCC), said mesh comprising first bias lines (PIX-VCC line to active pixel sensor pertaining to row-selects 322-2 and 322-4) disposed in a first direction which is substantially parallel (324-1, i.e., row-select) to said gate lines and second bias (PIX-VCC line to active pixel sensor pertaining to row-selects 322-1 and 322-3) lines disposed in a second direction which is substantially perpendicular to said gate lines and wherein a total length of said first bias lines exceeds a total length of said second bias lines. (See Fig. 8).

Regarding claim 21, Merrill shows in Fig. 8 that said total length of said first bias lines greatly exceeds said total length of said second bias lines by a factor of at least 10 times, and wherein said first bias lines are proximate to corresponding said gate lines (first bias lines comprise a path substantially greater than the second bias lines, see Fig. 8).

Regarding claim 22, Merrill shows in Fig. 8 a method for manufacturing a photodetecting array, said method comprising: forming a plurality of detecting cells (active pixel sensors, paragraph 0047, lines 1-2) arranged in an array, each of said detecting cells comprising a photodiode (112); forming a plurality of gate lines (324-1 and 324-2, i.e., first and second row-select lines, paragraph 0049, lines 1-5) coupled to said plurality of detecting cells; forming a plurality of data lines (326-1 and 326-2, i.e.,

column out lines) coupled to said plurality of detecting cells; forming a mesh of bias voltage lines (PIX-VCC), said mesh comprising first bias (PIX-VCC line to active pixel sensor pertaining to row-selects 322-2 and 322-4) lines disposed in a first direction which is substantially parallel to and proximate to said gate lines and second bias (PIX-VCC line to active pixel sensor pertaining to row-selects 322-1 and 322-3) lines disposed in a second direction which is substantially perpendicular to said gate lines and wherein a total length of said first bias lines exceeds a total length of said second bias lines (first bias lines comprise a path substantially greater than the second bias lines, see Fig. 8).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 3, 5, 8, 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Merrill (Publication No. U.S. 2002/0036700 A1) in view of Applicant's Admitted Prior Art (in Fig. 1).

Regarding claims 5 and 18, Merrill discloses the claimed invention as stated above. Merrill does not disclose that said photodiode in a cell is disposed above said transistor in said cell. Applicant's Admitted Prior Art shows in Fig. 1 that said photodiode

(99) in a cell is disposed above said transistor (35) in said cell. It would have been obvious to one skilled in the art to apply the pixel structure of Applicant's Admitted Prior Art to the device of Merrill for the purpose of providing maximum exposure to light to improve photodetection.

Regarding claims 3, 8 and 19, Merrill discloses the claimed invention as stated above. Merrill does not disclose that said photodiode comprises: an n+ layer formed over a first passivation layer; an amorphous silicon layer formed over said n+ layer; a p+ layer formed over said amorphous silicon layer; and a conductive layer formed over said p+ layer. Applicant's Admitted Prior Art shows in Fig. 1 that said photodiode comprises: an n+ layer (55) formed over a first passivation layer (40, i.e., SiON); an amorphous silicon layer (60, i.e., SiH) formed over said n+ layer (55); a p+ layer (65) formed over said amorphous silicon layer (60, i.e., SiH); and a conductive layer (70) formed over said p+ layer (65). It would have been obvious to one skilled in the art to apply the pixel structure of Applicant's Admitted Prior Art to the device of Merrill for the purpose of providing maximum exposure to light to improve photodetection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Goto (Publication No. U.S. 2002/0005474 A1) discloses a solid-state imaging system.

Mei (U.S. Patent No. 6,252,215 B1) discloses a hybrid sensor pixel architecture with gate line and drive line synchronization.

Orava (Publication No. U.S. 2001/0001562 A1) discloses imaging device system and method.

Sakurai (Publication No. U.S. 2003/0117510 A1) discloses an imaging pickup apparatus.

Yamashita (Publication No. U.S. 2002/0036257 A1) discloses an image pickup apparatus.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Wyatt whose telephone number is (571)-272-5974. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on (571)-272-2328. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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